In re Patent Application of:
LO IACONO
Serial No. 10/651,075
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REMARKS

Applicant would like to thank the Examiner for the thorough examination of the present application, and for allowing Claims 71-74. The Examiner rejected Claims 39-55 as being indefinite. In particular, the Examiner has taken the position that the claim recitation of "incrementing, decrementing or two's complementing a first string of N bits" is not supported by the current claims for providing the detailed steps/physical structure necessary to perform theses steps. The Examiner indicated that Claims 39-70 would be allowed upon overcoming the indefinite rejection.

Independent Claims 39 and 55 have been amended to more clearly define the present invention. In particular, independent Claim 39, for example, has been amended to recite "generating an output string as a logic combination of the auxiliary string and of the first string, the output string corresponding to the incrementing, decrementing or two's complement based on the logic combination used for generating the auxiliary string." Independent Claim 55 has been similarly amended.

The Examiner has taken the position that independent Claims 39 and 55 correspond to FIGS. 6A and 6B, which show only two's complement circuits; and consequently, the independent claims do not perform the incrementing and decrementing functions as claimed.

Referring to FIGS. 6A and 6B, the auxiliary string is respectively represented by M or $\overline{M}$, and the first string is represented by X. Independent Claim 39 recites that a logic combination is performed when generating the auxiliary string.

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Based upon the results of the logic combination (the logic
combination could be an OR mask or an AND mask as respectively
shown in FIGS. 6A and 6B, for example). The logic combination
used for generating the auxiliary string determines if an
incrementing, decrementing or two's complementing is being
performed. In this case, FIGS. 6A and 6B illustrate a two's
complement being performed. Dependent Claims 43 and 44 are
respectively directed to different embodiments of the two's
complement logic combination used in generating the auxiliary
string, i.e., the OR mask and the AND mask.

 The output string (represented by Y) is generated as a
logic combination of the auxiliary string and of the first
string. The logic combination for generating the output string Y
may be the same when generating the "incrementing, decrementing
or two's complementing the first string of N bits" as will also
be discussed below.

 One embodiment for the decrementing circuit is shown in
FIG. 9B, for example. The difference is the inverter in the
auxiliary string path. In other words, the logic combination
used for generating the auxiliary string is different in this
embodiment. Dependent Claims 45 and 46 are respectively directed
to different embodiments of the decrementing. However, the logic
combination used for generating the output string Y is the same
as in FIGS. 6A and 6B.

 A similar comparison can be made for the incrementing.
One embodiment for the incrementing circuit is shown in FIG. 10C,
for example. The difference is the two inverters in the
auxiliary string path. Dependent Claims 47 and 48 are

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respectively directed to different embodiments of the
<u>incrementing</u>. However, the logic combination used for generating
the output string Y is the same as in FIGS. 6A and 6B.

The Applicant submits that the independent claims
broadly recite generating the auxiliary string. Based on how the
auxiliary string is generated determines if incrementing,
decrementing or two's complementing of the N bit string is being
performed when generating the output string. Accordingly, the
Applicant submits that the claims are definite.

In view of the claim amendments and remarks provided
herein, it is submitted that all the claims are patentable.
Accordingly, a Notice of Allowance is requested in due course.
Should any minor informalities need to be addressed, the Examiner
is encouraged to contact the undersigned attorney at the
telephone number listed below.

Respectfully submitted,

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